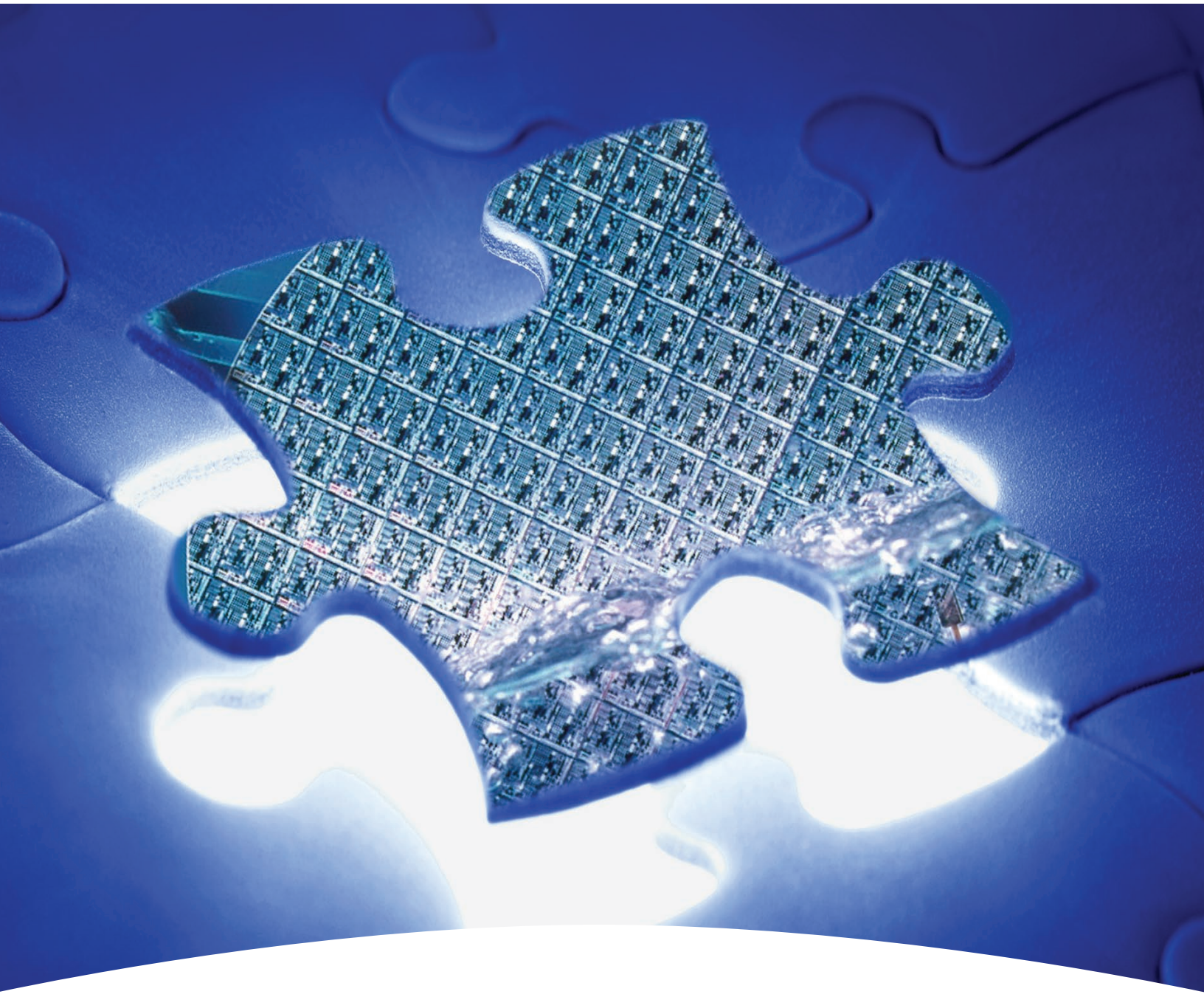
Electronic Chemicals

Honeywell



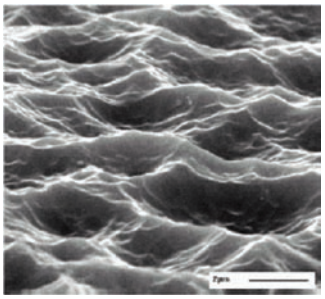
Honeywell Texture Etch for Wafer Thinning

Honeywell Texture Etch

WAFER THINNING MATERIALS

APPLICATIONS

- Increases surface area with uniform dimples to promote improved back-metal tensile strength
- Typical dimple depth is 0.00003 inch (8,000Å / 0.8µm)



15,000X

OVERVIEW

Honeywell's wafer thinning materials are part of three new product lines (wafer thinning materials, performance cleans, selective etchants) being introduced from its state-of-the-art electronic chemicals manufacturing sites in Chandler, Arizona and Seelze, Germany.

Honeywell's electronic chemicals manufacturing site in Chandler, Arizona.

These customized, application specific offerings provide improved cost of ownership (CoO), increased yield and ease-of-use. Our application expertise maximizes customer wafer thinning processes with application development support and troubleshooting know-how while our consistent drum-to-drum and bottle-to-bottle wafer etching characteristics provide unsurpassed batch-to-batch product uniformity. A robust manufacturing infrastructure and application expertise further enable Honeywell to deliver flexible end products, custom-matched to the best chemistry formulations for customer processes and specifications.

RESEARCH AND DEVELOPMENT

Honeywell and SEZ developed and performed an extensive design of experiment (DOE) to identify the critical chemical and operating parameters for surface roughness, etch uniformity and etch rate of a silicon texture process, during the preparation of the wafer for back-metal (utilizing a SEZ single wafer processing tool).

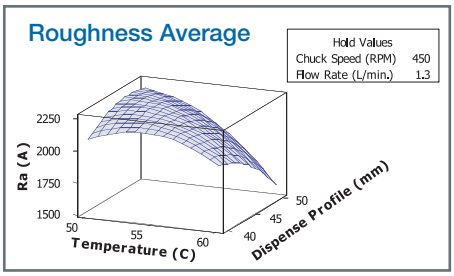
ETCHER PARAMETER	SETTING		
	High	Middle	Low
Temperature (°C)	60	55	50
Chuck Speed (RPM)	600	450	300
Flow Rate (L/min.)	1.6	1.3	1.0
Dispense Profile (mm)	50	45	40

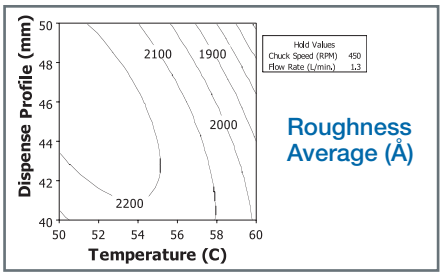
A stable etch process and consistent etchant are needed to ensure a stable wafer backside etching process

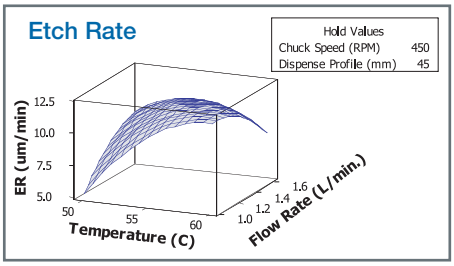
Conclusions of this work indicate:

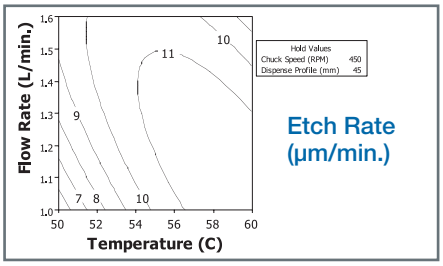
- **Post etch surface roughness** is primarily a function of the **dispense profile and temperature**
- The silicon **etch rate** is primarily a function of **temperature**
- The silicon **etch uniformity** is primarily a function of the **temperature and flow rate**

(See Roughness and Etch Rate data below.)









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